

Patent Assignment Abstract of Title

Total Assignments: 1**Application #:** 09703792 **Filing Dt:** 11/02/2000 **Patent #:** NONE **Issue Dt:****PCT #:** NONE **Publication #:** NONE **Pub Dt:****Inventors:** Shinji Hayakawa, Satoshi Watanabe, Atsushi Shimbo, Hiromi Aoyagi**Title:** Packet receiver with the influence of jitter and packet losses reduced before a buffer becomes idle due to data delays and packet receiving method using the same**Assignment: 1**

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		11/27/2000	11/02/2000	01/27/2001	5

Conveyance: ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS).**Assignors:** HAYAKAWA, SHINJI**Exec Dt:** 10/04/2000WATANABE, SATOSHI**Exec Dt:** 10/04/2000SHIMBO, ATSUSHI**Exec Dt:** 10/06/2000AOYAGI, HIROMI**Exec Dt:** 10/06/2000**Assignee:** OKI ELECTRIC INDUSTRY, CO. LTD.

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<u>L29</u>	L28 and (L25 or L18 or L2)	4	<u>L29</u>
<u>L28</u>	(absorb\$6 near1 jitter\$)	236	<u>L28</u>
<u>L27</u>	dummy and L25	0	<u>L27</u>
<u>L26</u>	L1 and L25	1	<u>L26</u>
<u>L25</u>	6658027.pn. or 5914936.pn.	2	<u>L25</u>
<u>L24</u>	dummy and L19	1	<u>L24</u>
<u>L23</u>	(buffer\$6 or queue\$6 or memory or memor\$6) and L22	5	<u>L23</u>
<u>L22</u>	(speech same delay\$6) same L16	5	<u>L22</u>
<u>L21</u>	(speech same delay\$6) and L18	3	<u>L21</u>
<u>L20</u>	(decod\$6 near4 (speech or data)) same L16	1	<u>L20</u>
<u>L19</u>	decod\$6 and L18	4	<u>L19</u>
<u>L18</u>	L1 and L16	28	<u>L18</u>
<u>L17</u>	L16 and (L4 or L2)	1	<u>L17</u>

<u>L16</u>	discard\$6 same L14	126	<u>L16</u>
<u>L15</u>	L2 and L14	5	<u>L15</u>
<u>L14</u>	exceed\$6 near4 (delay\$6 or jitter\$)	7057	<u>L14</u>
<i>DB=USPT; PLUR=YES; OP=ADJ</i>			
<u>L13</u>	'6434606'.pn.	1	<u>L13</u>
<u>L12</u>	'6452950'.pn.	1	<u>L12</u>
<u>L11</u>	'6452950'.pn.	1	<u>L11</u>
<u>L10</u>	'6434606'.pn.	1	<u>L10</u>
<u>L9</u>	'6434606'.pn.	1	<u>L9</u>
<i>DB=PGPB,USPT; PLUR=YES; OP=ADJ</i>			
<u>L8</u>	discard\$6 and L7	4	<u>L8</u>
<u>L7</u>	threshold\$ and L6	5	<u>L7</u>
<u>L6</u>	(jitter\$ same delay\$6) and L4	8	<u>L6</u>
<u>L5</u>	(threshold\$ same discard\$6) and L4	0	<u>L5</u>
<u>L4</u>	6389032.uref.	10	<u>L4</u>
<u>L3</u>	L2 and L1	5	<u>L3</u>
<u>L2</u>	4607363.uref. or 6389032.uref.	26	<u>L2</u>
<u>L1</u>	(buffer\$6 or queue\$6 or memory or memor\$6) same threshold\$ same discard\$6	1571	<u>L1</u>

END OF SEARCH HISTORY